CLAIMS

What is claimed is:

1. An apparatus, comprising:

a plurality of tag units, each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations;

a memory module decode unit, the memory module decode unit to perform decode operations in parallel with the tag look-up operations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a plurality of data caches, each data cache associated with one of a plurality of memory modules.

2. The apparatus of claim 1, each of the plurality of tag units corresponding to one of the plurality of memory modules.

3. The apparatus of claim 2, the tag look-up operations to provide cache hit information.

4. The apparatus of claim 3, the tag look-up operations to provide cache line modified information.

5. The apparatus of claim 4, each of the arrays of tag address storage locations organized into a plurality of ways.

6. The apparatus of claim 5, the tag look-up operations to provide way information.

7. The apparatus of claim 6, each of the arrays of tag address storage locations organized into 4 ways

8. The apparatus of claim 1, the command sequencer and serializer unit to control the plurality of data caches associated with the plurality of memory modules by delivering commands over a plurality of command and address lines.

9. The apparatus of claim 8, wherein the plurality of command and address lines are part of a point-to-point interconnect.

10. A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

a plurality of tag units, each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations;

a memory module decode unit, the memory module decode unit to perform decode operations in parallel with the tag look-up operations; and

a command sequencer and serializer unit coupled to the array of tag

address storage locations; and

a plurality of memory modules coupled to the memory controller, each of the plurality of memory modules including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by

commands delivered by the memory controller.

11. The system of claim 10, a point-to-point interconnect to couple the memory controller to the memory modules.

12. The system of claim 11, the arrays of tag address storage locations and the data caches organized into a plurality of ways.

13. The system of claim 12, the tag look-up operations to provide cache hit information.

14. The system of claim 13, the tag look-up operations to provide cache line modified information.

15. The system of claim 14, the tag look-up operations to provide way information.

16. A method, comprising:

receiving a read request at a memory controller;

performing a tag look-up within the memory controller to determine whether there is a cache hit for the read request;

determining which of a plurality of memory modules is addressed by the read request, wherein performing a tag look-up and determining which of a plurality of memory modules is addressed by the read request occur in parallel; and

fetching a line of cache data from a data cache located on one of the plurality of memory modules if the tag look-up indicates a cache hit.

17. The method of claim 16, wherein performing a tag look-up includes providing way information.

18. The method of claim 17, wherein performing a tag look-up operation includes providing cache line modified information.